REMARKS

Amendments to the Specification

As directed in the office action summary, the following corrections were made to the specification. No new matter was added in the performed amendments.

In the Title:

Title has been amended to "OPTICAL RECORDING SYSTEM WITH A BUILT-IN JITTER DETECTOR" to more accurately describe the subject matter of the present invention as suggested by the Examiner.

In the Abstract: typographical error

A typographical error reading "anda" was corrected to "and a" as suggested by the Examiner.

Response to Claim rejections

Rejection of Claim 12 under U.S.C. 112 as being indefinite for failing to particularly point out and distinctly claim the subject mater which applicant regards as the invention

Claim 12 has been amended to more distinctly point out and claim the subject matter of the present invention. Claim 12 is fully supported in the original disclosure with no additional subject matter added. The limitation for currently amended claim 12 is disclosed in paragraph 17 of the detailed description, reading "The write strategy needs to be fine tuned according to the material and manufacturer of the optical disc 26". Reconsideration of Claim 12 is respectfully requested.

Rejection of Claim 1 under U.S.C. 102(a) as being anticipated by Nakajima et al.

(US 2001/0006500A1)

In regards to Claim 1, applicant has amended Claim 1 to include all the limitations of Claim 2 and Claim 3, as was stated would be allowable by the Examiner. Claims 2 and 3 are correspondingly cancelled, and the Claim 4 is amended to be dependent upon Claim 1. Applicant asserts that as Claim 3 is in a state of allowance, it's merger into base Claim 1 with intervening Claim 2 should therefore place Claim 1 in a state of allowance. Applicant kindly requests the Examiner re-evaluate currently amended Claim 1 in consideration for its allowance.

Rejection of Claim 2 under U.S.C. 102(a) as being anticipated by Nakajima et al. (US 2001/0006500A1)

As mentioned above, applicant has merged all the limitations of Claim 2 and Claim 3 into Claim 1, as was stated would be allowable by the Examiner.

Rejection of Claims 4-7 under U.S.C. 102(a) as being anticipated by Nakajima et al. (US 2001/0006500A1)

Regarding Claims 4-7, applicant points out that these claims are dependant upon amended base Claim 1, which was amended to place it in a state of allowance according to limitations found allowable by the Examiner. Therefore, should an allowance be made for Claim 1, applicant kindly requests that allowances be similarly made for Claims 4-7 being dependent upon Claim 1.

Rejection of Claim 8 under U.S.C. 102(a) as being anticipated by Nakajima et al. (US 2001/0006500A1)

Claim 8 has been amended to follow newly amended Claim 1 as its corresponding method claim. Claim 8 therefore has been amended to include all the limitations disclosed in Claims 9 and 10, and additionally to state "the delay signal is formed by a plurality of delay bits received from a plurality of buffers, each buffer connected to a delay cell". This additional limitation corresponds to Claim 3 (which is in a state of allowance) in a method format, and is fully supported in the original disclosure in paragraph 21 stating " the buffer set 44 stores an 8-bit delay signal transmitted from the eight delay cells 42 of the delay chain 48". No new subject matter is introduced in these amendments.

Applicant asserts that providing a delay signal formed by a plurality of delay bits received from a plurality of buffers, each buffer being connected to a delay cell, contrasts the teachings of Nakajima et al. Fig. 10 of Nakajima et al. shows the delay cells (DFF_{11}-DFF_{15}) separated from the buffers (DFF_{16}, DFF_{17}). Therefore, it is clear that Nakajima et al. do not teach connecting each buffer directly to a delay cell for providing a delay bit.

Rejection of Claims 9,10 under U.S.C. 102(a) as being anticipated by Nakajima et al. (US 2001/0006500A1)

In regards to Claims 9 and 10, applicant has merged the limitations of Claims 9 and 10 into Claim 8, and has subsequently canceled Claims 9 and 10.

Rejection of Claims 11,12 under U.S.C. 102(a) as being anticipated by Nakajima et al. (US 2001/0006500A1)

Regarding Claims 11 and 12, applicant points out that these claims are dependant upon amended base Claim 8, which was amended to place it in a state of allowance according to limitations found allowable by the Examiner. Therefore, should an allowance be made for Claim 8, applicant kindly requests that allowances be similarly made for Claims 11 and 12 being dependent upon Claim 8.

Introduction of New Claims 13-16

Applicant has introduced new Claims in order to distinctly claim additional features and alternative embodiments of the present invention.

Regarding Claim 13, Claim 13 introduces an optical recording system including a jitter meter. The jitter meter includes a delay chain with a plurality of delay cells connected in a cascade manner, wherein a processed RF signal is coupled to a clock input of the first delay cell, and the output of each delay cell is coupled to a clock input of the following delay cell. This aspect is fully supported in Fig. 3 and paragraph 19 of the original disclosure stating "The clock input of the first delay cell 42 is connected to the read channel 20 for receiving the processed RF signal. The clock input of each of the

remaining delay cells 42 is connected to the output Q of a previous delay cell 42". When an input is connected to the input of each delay cell, this structure allows the input to be delayed according to the processed RF signal. A delay signal can then be determined according to the delayed RF signal and the control signal.

Applicant asserts that Nakajima et al. do not teach a delay chain with a plurality of delay cells connected in a cascade manner, wherein a processed RF signal is coupled to a clock input of the first delay cell, and the output of each delay cell is coupled to a clock input of the following delay cell. Fig. 10 of Nakajima et al. show that delay cells (DFF_{11}-DFF_{15}) are simply connected in series, with each delay cell sharing an identical clock signal. Using this structure, Nakajima teaches a method where the input signal Abs is alternatively delayed incrementally from each delay cell at every edge of a shared driving clock signal.

Regarding Claim 14, it describes the buffer set comprising a plurality of buffers each connected to a delay cell for receiving a delay bit of the delay signal transmitted from the delay cell. This contrasts the teachings of Nakajima et al, as Fig. 10 of Nakajima illustrates buffers (DFF_{16},DFF_{17}) being electrically separated from the delay cells (DFF_{11}-DFF_{15}), and having additional hardware components between them. Applicant asserts that the buffers of Nakajima cannot each receive a delay bit from a delay cell as the hardware layout of Nakajima prevents this occurrence.

Regarding Claims 15 and 16, these claims are method claims analogous to system Claims 15 and 16. Consideration of new Claims 13-16 is respectfully requested.

Sincerely yours,

Winston Hsu Date: 04/19/2006

Winston Hsu, Patent Agent No. 41,526
P.O. BOX 506, Merrifield, VA 22116, U.S.A.
Voice Mail: 302-729-1562
Facsimile: 806-498-6673
e-mail : winstonhsu@naipo.com

Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)